SSC8113GS6

P-Channel Enhancement Mode MOSFET

➢ Features

V_{DS}	V_{GS}	$R_{DS(ON)}$ Typ.	I_D
-16V	±12V	46mΩ@-4V5	-4A
		60mΩ@-2V5	

➢ Description

This device is produced with high cell density DMOS trench technology, which is especially used to minimize on-state resistance. This device particularly suits low voltage applications such as portable equipment, power management and other battery powered circuits, and low in-line power dissipation are needed in a very small outline surface mount package.

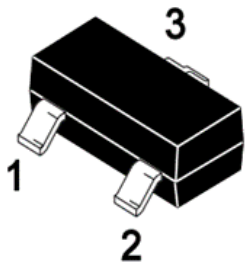
➢ Applications

- Load Switch
- Portable Devices
- DCDC Conversion

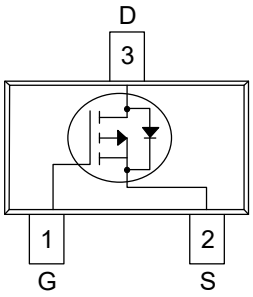
➢ Ordering Information

Device	Package	Shipping
SSC8113GS6	SOT-23	3000/Reel

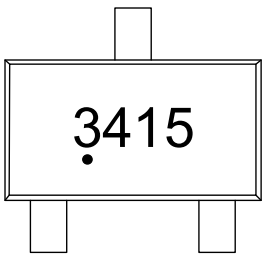
➢ Pin configuration



SOT-23



Pin Configuration (Top View)



Marking

➢ Absolute Maximum Ratings (T_A=25℃ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	-16	V
V_{GSS}	Gate-to-Source Voltage	±12	V
I_D	Continuous Drain Current [a]	-4	A
I_{DM}	Pulsed Drain Current [b]	-15	A
P_D	Power Dissipation [c]	0.98	W
P_{DSM}	Power Dissipation [a]	0.57	W
T_J	Operation junction temperature	-55~150	℃
T_{STG}	Storage temperature range	-55~150	℃

➢ Thermal Resistance Ratings (T_A=25℃ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance [a]	220	℃/W
$R_{\theta JC}$	Junction-to-Case Thermal Resistance	128	

Note:

a. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz.copper, in a still air environment with T_A=25℃.The value in any given application depends on the user is specific board design. The power dissipation is based on the t≤10s thermal resistance rating.

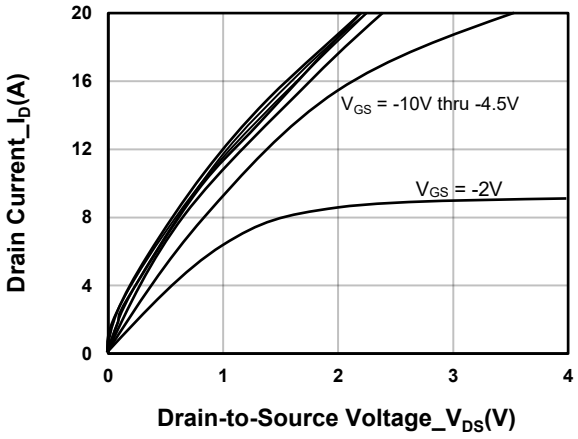
b. Repetitive rating, pulse width limited by junction temperature.

c. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

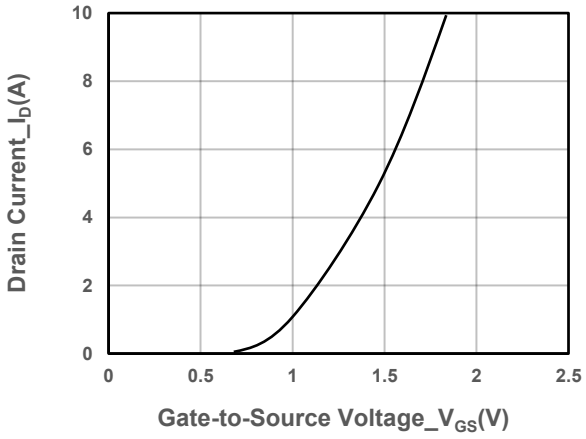
➢ Electrical Characteristics (T_A=25℃ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-16			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250uA	-0.4	-0.65	-1	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -4.5V, I_D = -2A		46	59	mΩ
		V_{GS} = -2.5V, I_D = -1A		60	78	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -12V, V_{GS} = 0V			-1	μA
Gate-Source Leak Current	I_{GSS}	V_{GS} = ±12V, V_{DS} = 0V			±100	nA
Forward Voltage	V_{SD}	V_{GS} = 0V, I_S = -1A			-1.3	V
Input Capacitance	C_{ISS}	V_{DS} = -10V, V_{GS} = 0V, f = 1MHz		550		pF
Output Capacitance	C_{OSS}			70		
Reverse Transfer Capacitance	C_{RSS}			55		
Turn-on Delay Time	$T_{D(ON)}$	V_{DS} = -10V, V_{GS} = -4.5V, R_{GEN} = 3Ω, I_D = -2A		6		ns
Rise Time	T_r			22		
Turn-off Delay Time	$T_{D(OFF)}$			38		
Fall Time	T_f			45		
Total Gate Charge	Q_G	V_{GS} = -4.5V, V_{DS} = -10V, I_D = -2A		5.8		nC
Gate to Source Charge	Q_{GS}			1.2		
Gate to Drain Charge	Q_{GD}			1		

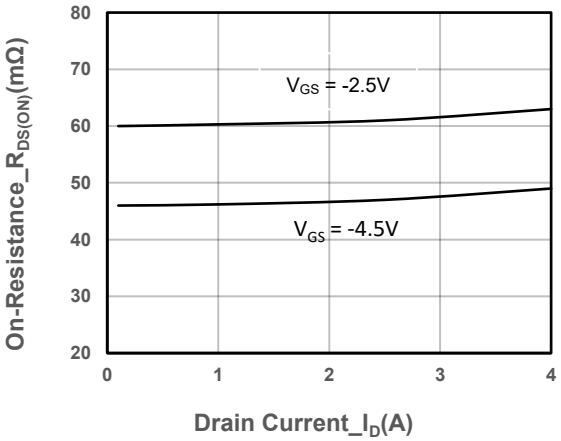
➢ Typical Performance Characteristics (T_A=25℃ unless otherwise noted)



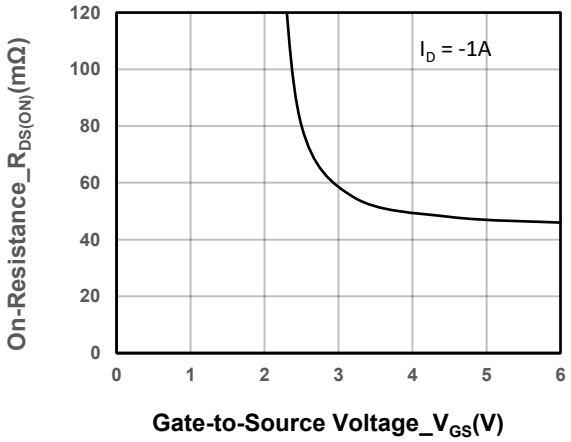
Output Characteristics



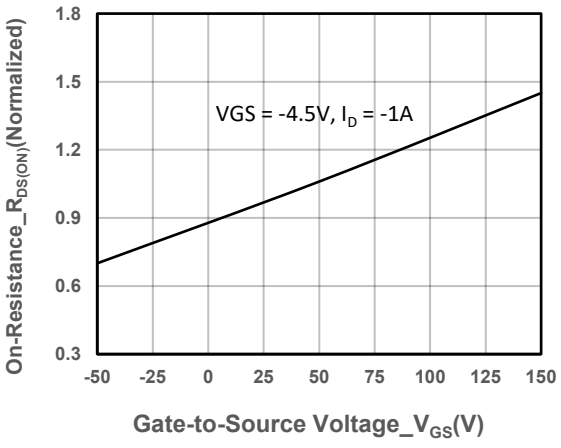
Transfer Characteristics



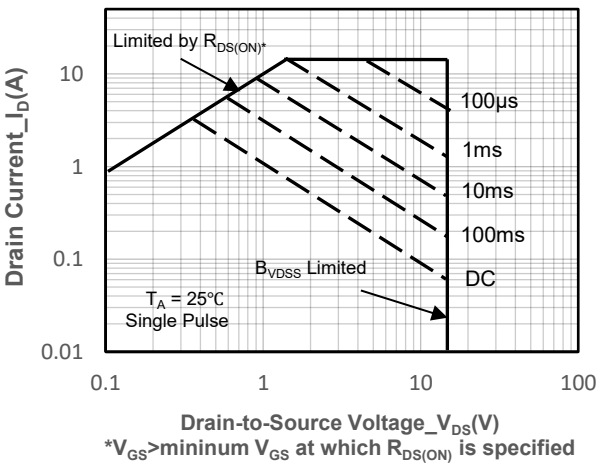
On-Resistance vs. Drain Current and Gate Voltag



On-Resistance vs. Gate-to-Source Voltage

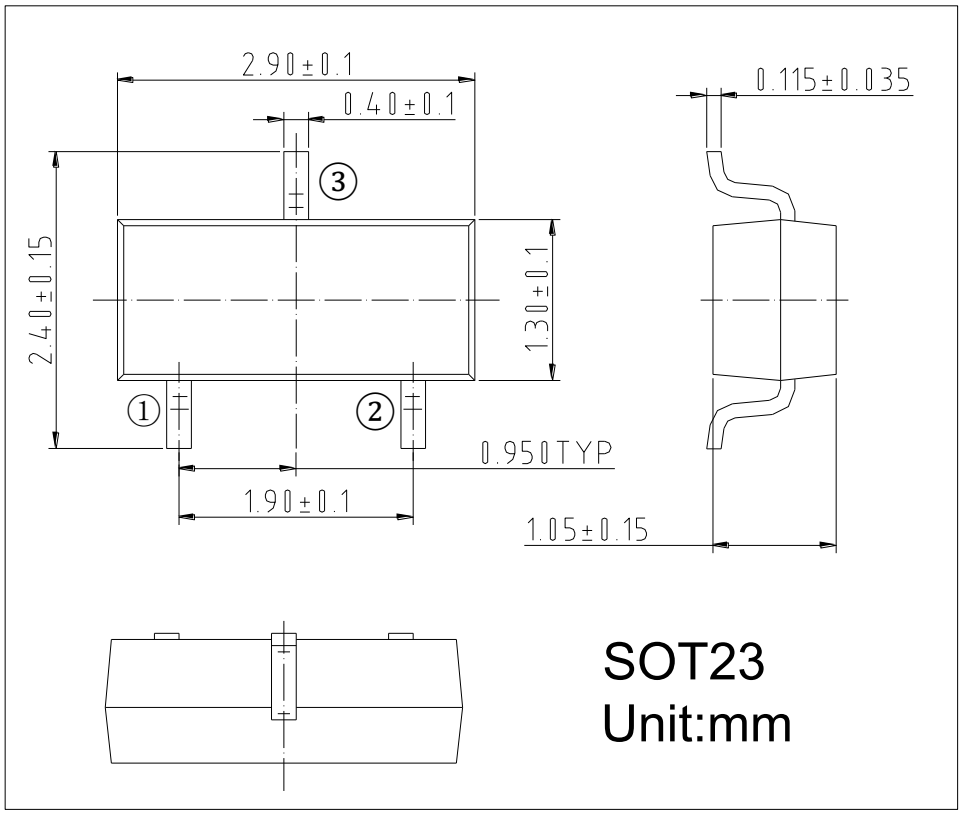


On-Resistance vs. Junction Temperature

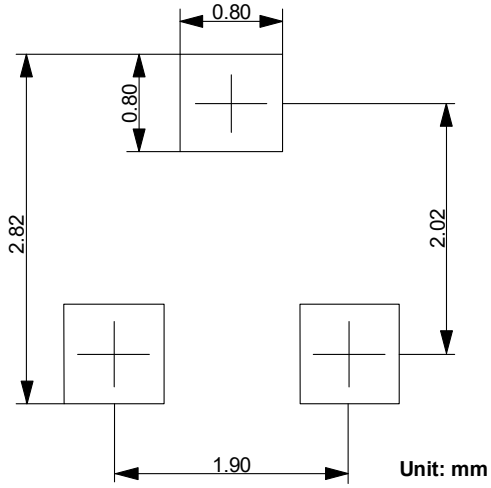


Safe Operating Area vs. Junction-to-Ambient

➢ Package Information



➢ Recommended Pad outline



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